Chopper Stabilized Omnipolar Hall-Effect Switch

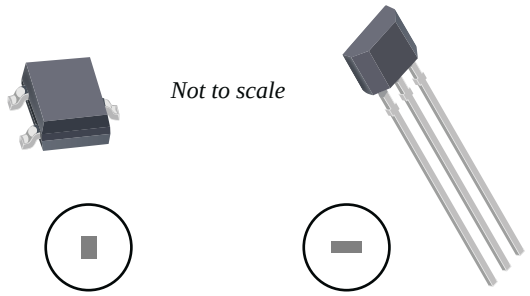
Features and Benefits

- Omnipolar operation
- Low switchpoint drift
- Superior temperature stability
- Insensitive to physical stress
- Reverse battery protection
- Robust EMC capability
- Robust ESD protection

Packages:

3-pin SOT23-W
2 mm × 3 mm × 1 mm
(suffix LH)

3-pin ultramini SIP
1.5 mm × 4 mm × 3 mm
(suffix UA)



Not to scale

Approximate footprint

Description

The A1126 integrated circuit is an omnipolar, ultrasensitive Hall-effect switch with a digital output. This device has an integrated regulator permitting operation to 24 V.

This device is especially suited for operation through extended temperature ranges, up to 150°C. Superior high-temperature performance is made possible through an Allegro® patented dynamic offset cancellation, which reduces the residual offset voltage normally caused by device overmolding, temperature excursions, and thermal stress.

The A1126 Hall-effect switch includes the following on a single silicon chip: voltage regulator, Hall-voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, and a short circuit protected open-drain output. Advanced BiCMOS wafer fabrication processing is used to take advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries.

The omnipolar operation of the A1126 allows activation with either a north or a south polarity field of sufficient strength. In the absence of a magnetic field, the output is off. This patented magnetic-polarity–independence feature makes this device an excellent replacement for reed switches, with improved ease of manufacturing, because the A1126 does not

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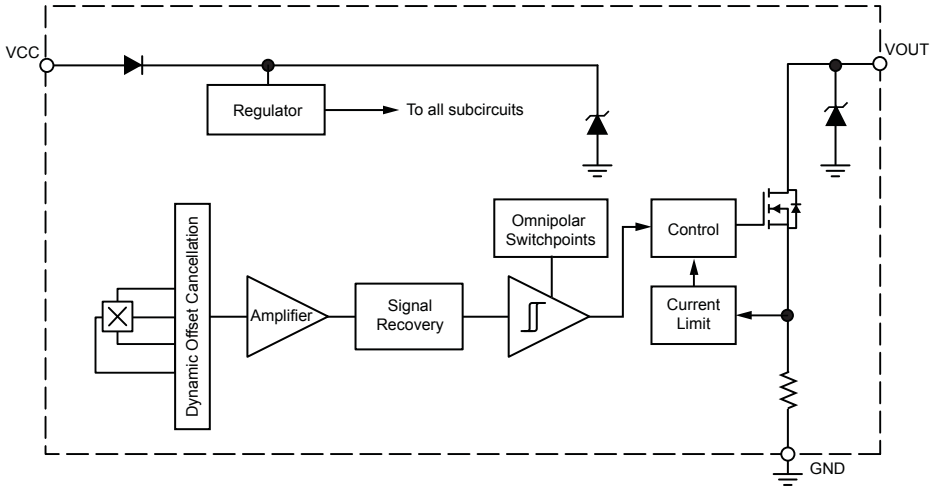
Functional Block Diagram



Description (continued)

require manufacturers to orient their magnets. These devices allow simple on/off switching in industrial, consumer, and automotive applications.

The A1126 is rated for operation between the ambient temperatures –40°C to 150°C. The available package styles provide magnetically optimized solutions for most applications. Package LH is an SOT23W, a miniature low-profile surface-mount package, while package UA is a three-lead ultramini SIP for through-hole mounting. Each package is lead (Pb) free, with 100% matte tin plated leadframe.

Selection Guide

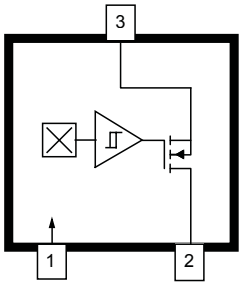
Part Number	Packing[1]	Package
A1126LLHLT-T[2]	3,000 pieces per reel	3-pin SOT-23W surface mount
A1126LLHLX-T	10,000 pieces per reel	3-pin SOT-23W surface mount
A1126LUA-T	500 pieces per bag	3-pin ultramini SIP through-hole mount

[1]Contact Allegro® for additional packing options
[2]Available through authorized Allegro distributors only.

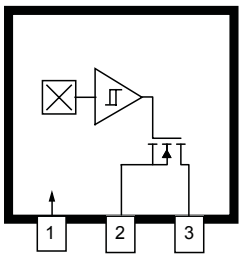
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Output Off Voltage	V_{OUT}		28	V
Reverse Supply Current	I_{RCC}		–2	mA
Continuous Output Current	I_{OUT}		Internally limited	–
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Pin-out Diagrams



LH Package
3-pin SOT23W



UA Package
3-pin SIP

Terminal List Table

Name	Number		Function
	LH	UA	
VCC	1	1	Connects power supply to chip
VOUT	2	3	Output from circuit
GND	3	2	Ground

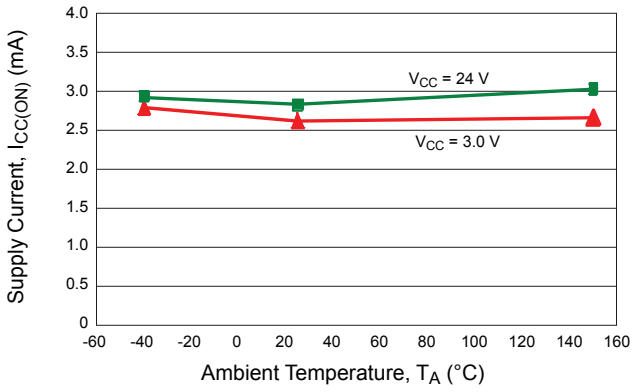
OPERATING CHARACTERISTICS Valid through T_A and V_{CC} ranges, $T_J < T_J(max)$, C_{BYP} = 0.1 µF; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Electrical Characteristics						
Supply Voltage	V_{CC}	Operating, T_J < 165°C	3	–	24	V
Output Leakage Current	I_{OUTOFF}	V_{OUT} = 24 V, B < B_{RPS}	–	–	10	µA
Output On Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	–	185	500	mV
Output Current Limit	I_{OM}	B > B_{OP}	30	–	60	mA
Power-On Time[2,3]	t_{PO}		–	–	25	µs
Chopping Frequency	f_C		–	800	–	kHz
Output Rise Time[3,4]	t_r	R_{LOAD} = 820 Ω, C_S = 20 pF	–	0.2	2	µs
Output Fall Time[3,4]	t_f	R_{LOAD} = 820 Ω, C_S = 20 pF	–	0.1	2	µs
Supply Current	$I_{CC(ON)}$	B > B_{OP}, V_{CC} = 12 V	–	–	4	mA
	$I_{CC(OFF)}$	B < B_{RP}, V_{CC} = 12 V	–	–	4	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = 6.5 mA; T_A = 25°C	28	–	–	V
Supply Zener Current	$I_{ZSUPPLY}$	V_S = 28 V	–	–	6.5	mA
Magnetic Characteristics						
Operate Point	B_{OPS}	South pole adjacent to branded face	15	38	55	G
	B_{OPN}	North pole adjacent to branded face	-55	-38	-15	G
Release Point	B_{RPS}	South pole adjacent to branded face	5	20	50	G
	B_{RPN}	North pole adjacent to branded face	-50	-20	-5	G
Hysteresis	B_{HYS}	$\lvert B_{OPS} - B_{RPS} \rvert$, $\lvert B_{OPN} - B_{RPN} \rvert$	5	–	30	G

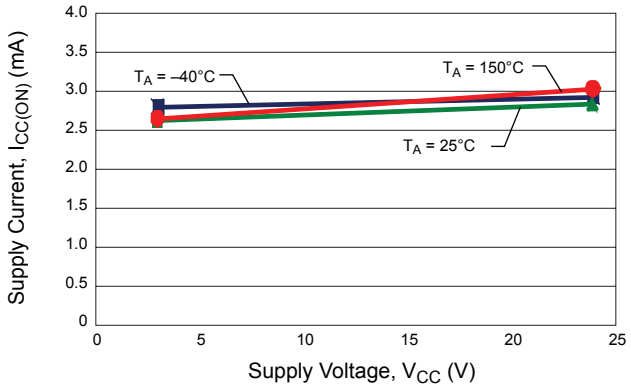
[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] B < B_{RP}(min) – 10 G , B > B_{OP}(max) + 10 G.
[3] Guaranteed by device design and characterization.
[4] C_S = oscilloscope probe capacitance.

Characteristic Performance

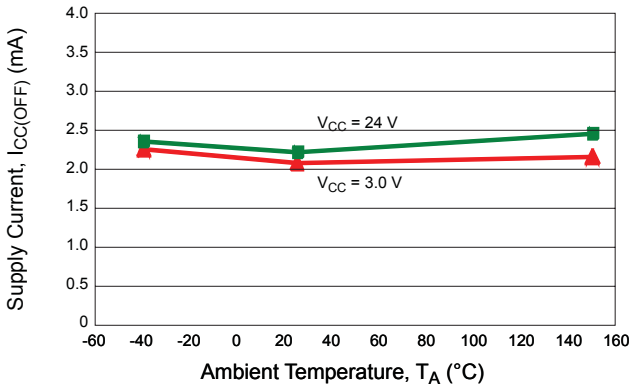
Average Supply Current (On) versus Temperature



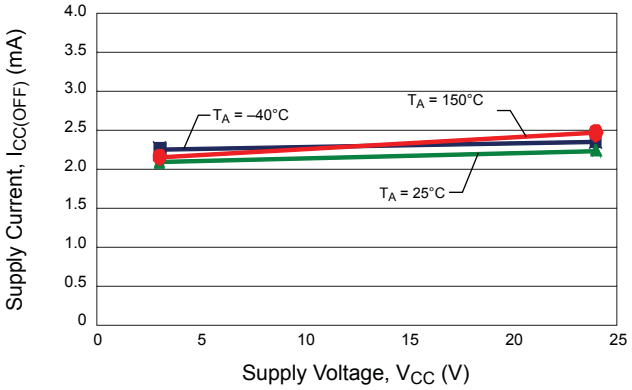
Average Supply Current (On) versus Supply Voltage



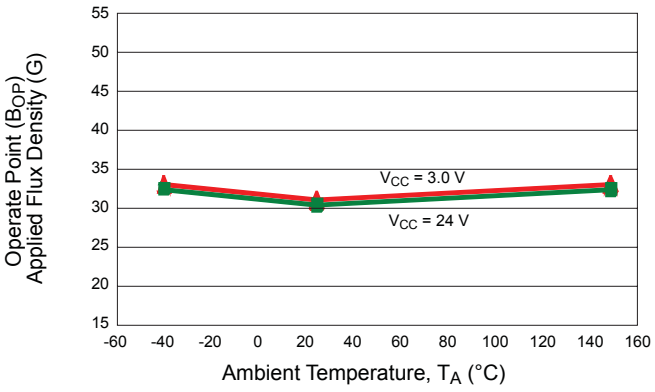
Average Supply Current (Off) versus Temperature



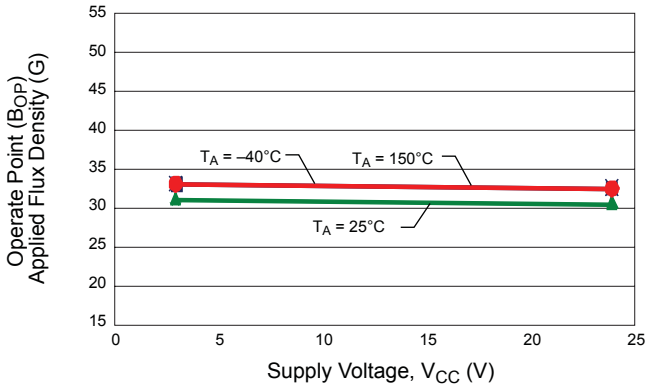
Average Supply Current (Off) versus Supply Voltage



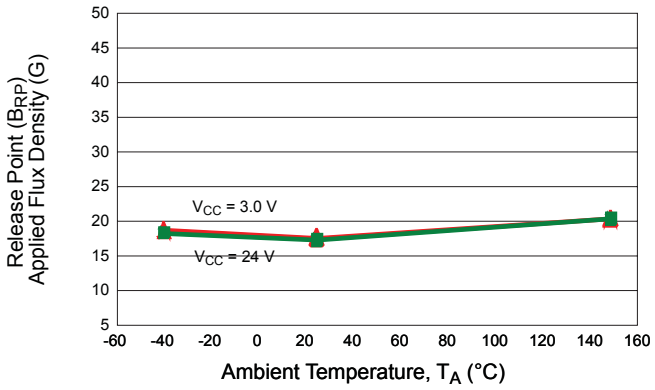
Average Operate Point (South) versus Temperature



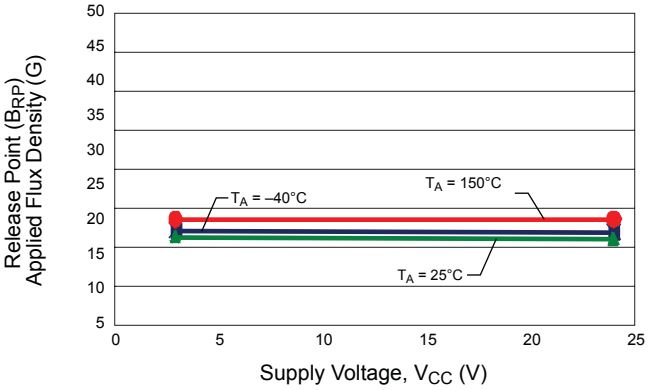
Average Operate Point (South) versus Supply Voltage



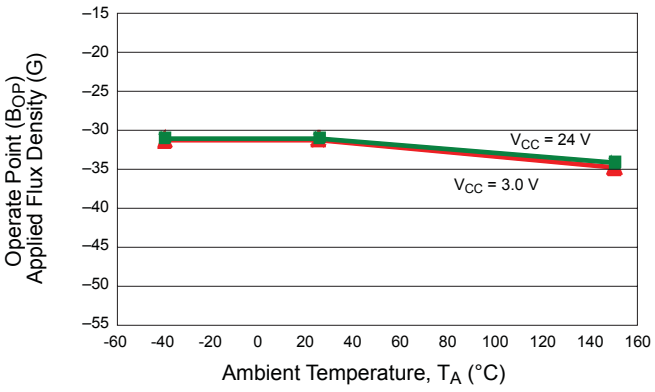
Average Release Point (South) versus Temperature



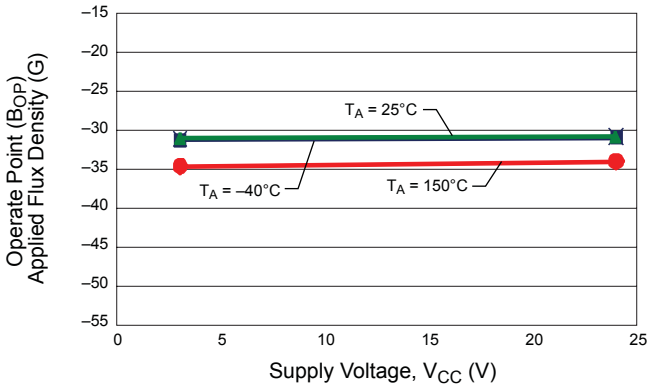
Average Release Point (South) versus Supply Voltage



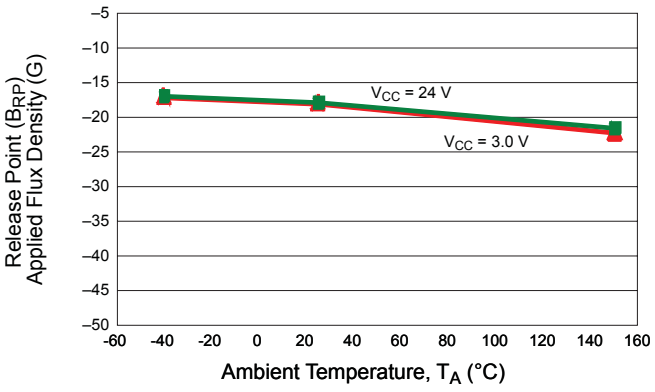
Average Operate Point (North) versus Temperature



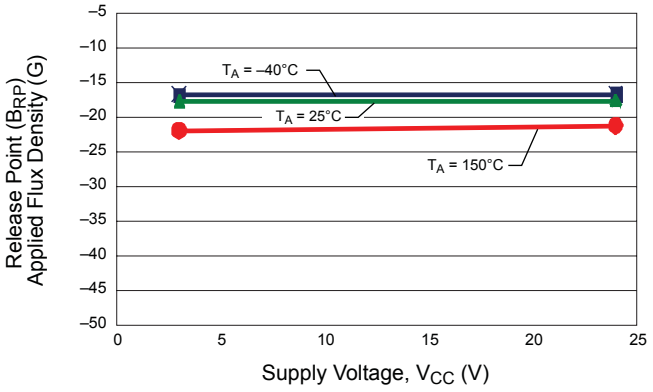
Average Operate Point (North) versus Supply Voltage



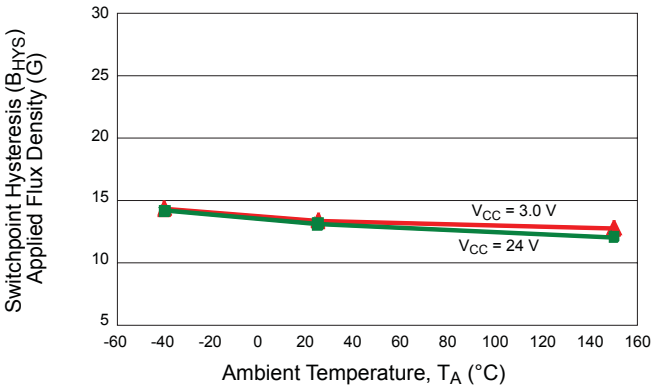
Average Release Point (North) versus Temperature



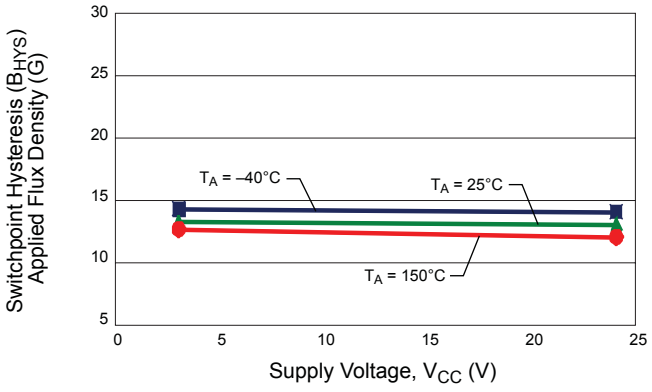
Average Release Point (North) versus Supply Voltage



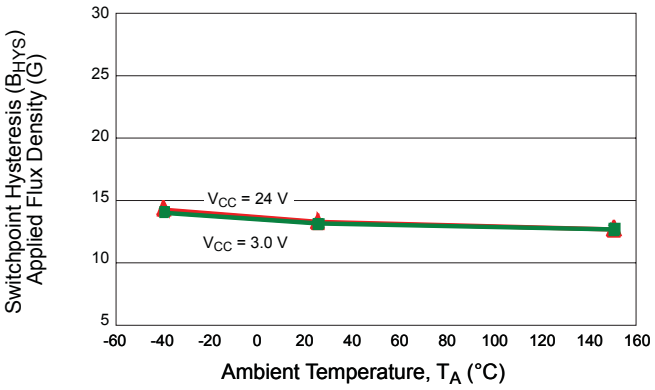
Average Hysteresis (South) versus Temperature



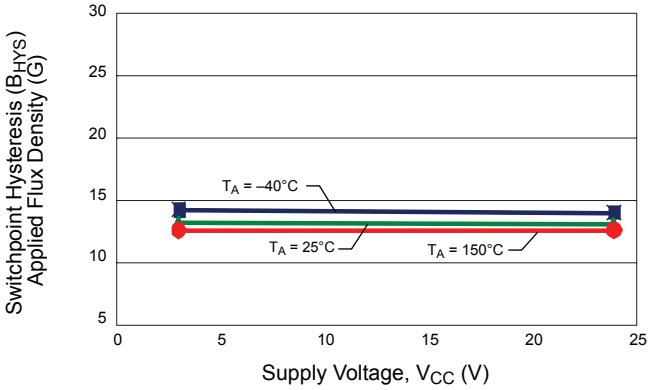
Average Hysteresis (South) versus Supply Voltage



Average Hysteresis (North) versus Temperature

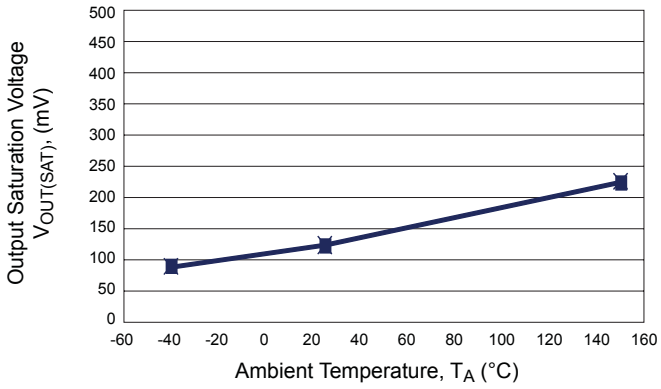


Average Hysteresis (North) versus Supply Voltage



Average Output Saturation Voltage versus Temperature

I_{OUT} = 20 mA, V_{CC} = 12 V, B > B_{OP}

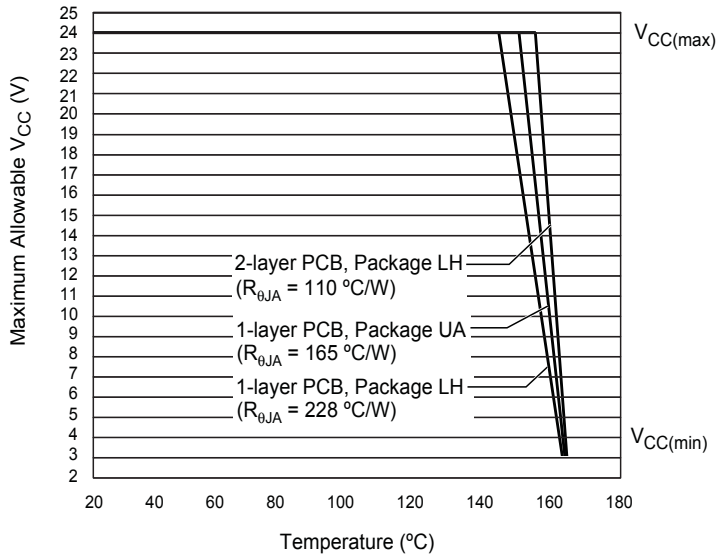


THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

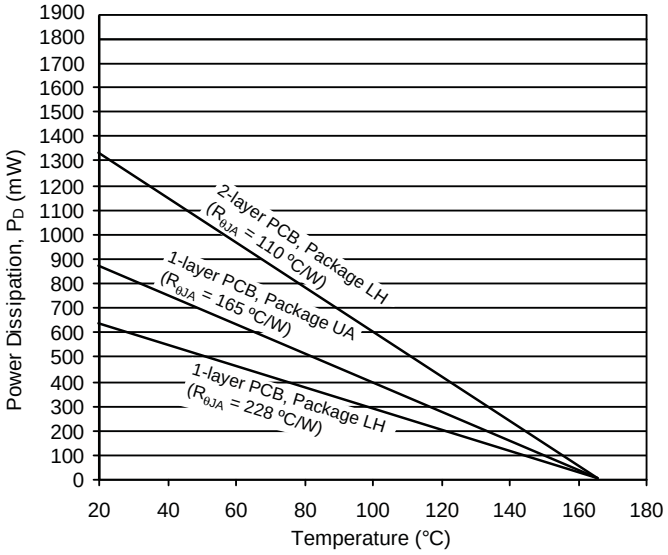
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	ºC/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	ºC/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W

*Additional thermal information available on Allegro Web site.

Power Derating Curve



Power Dissipation versus Ambient Temperature



Functional Description

The output of these devices switches low (turns on) when a magnetic field perpendicular to the Hall sensor chip exceeds the operate point threshold, B_{OPx}. After turn-on, the output voltage is $V_{OUT(SAT)}$. The output transistor is capable of sinking current up to the short circuit current limit, I_{OM}, which is a minimum of 30 mA. When the magnetic field is reduced below the release point, B_{RPx}, the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

In the case of omnipolar switch devices, removal of the magnetic field results in the device output high (off).

Powering-on the device in the hysteresis range (less than B_{OPx} and greater than B_{RPx}) will allow an indeterminate output state. The correct state is attained after the first excursion beyond B_{OPx} or B_{RPx}.

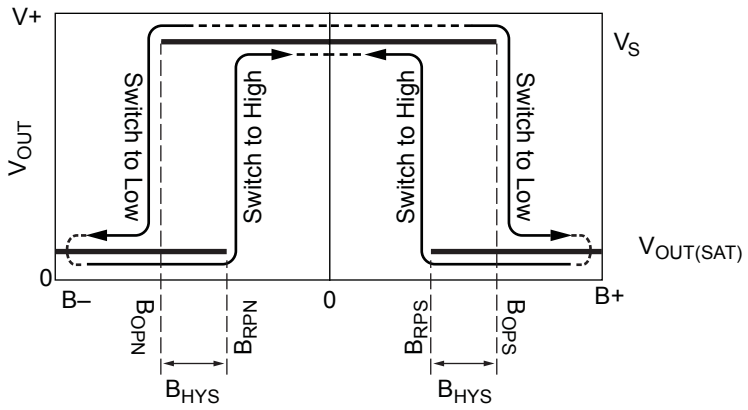


Figure 1. Switching behavior of omnipolar switches. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates increasing north polarity. This behavior can be exhibited when using a circuit such as that shown in figure 2.

Application Information

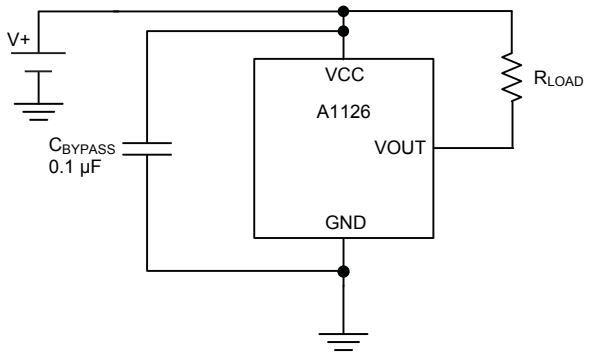


Figure 2. Typical Application Circuit

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor chip. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 400 kHz high frequency clock. For demodulation process, a sample-and-hold technique is used, where the sampling is performed at twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

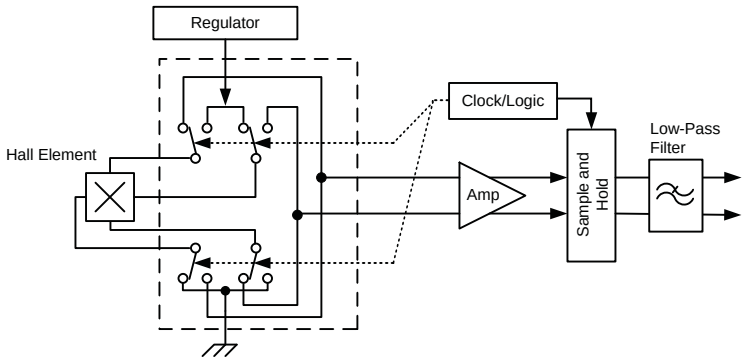


Figure 3. Concept of Chopper Stabilization Technique

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_J(max)$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{IN} = 12 V, I_{IN} = 4 mA, and $R_{\theta JA}$ = 140 °C/W, then:

$$P_D = V_{IN} \times I_{IN} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140\ °C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level, without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UA, using a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=165 °C/W, $T_J(max)$ =165°C, $V_{CC}(max)$ =24 V, and $I_{CC}(max)$ = 4 mA.

Calculate the maximum allowable power level, $P_D(max)$. First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165\ °C/W = 91\ mW$$

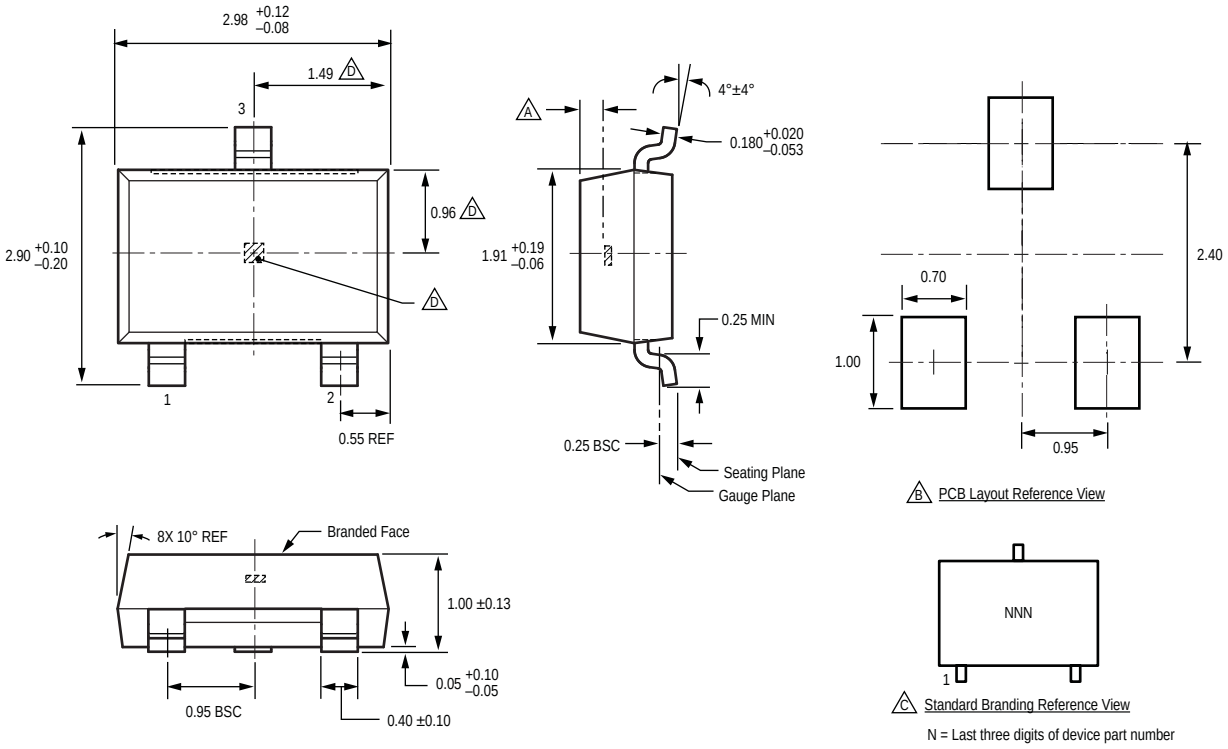
Finally, invert equation 1 with respect to voltage:

$$V_{CC}(est) = P_D(max) \div I_{CC}(max) = 91\ mW \div 4\ mA = 23\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC}(est)$.

Compare $V_{CC}(est)$ to $V_{CC}(max)$. If $V_{CC}(est) \leq V_{CC}(max)$, then reliable operation between $V_{CC}(est)$ and $V_{CC}(max)$ requires enhanced $R_{\theta JA}$. If $V_{CC}(est) \geq V_{CC}(max)$, then operation between $V_{CC}(est)$ and $V_{CC}(max)$ is reliable under these conditions.

Package LH, 3-Pin SOT23W



N = Last three digits of device part number

For Reference Only; not for tooling use (reference DWG-2840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

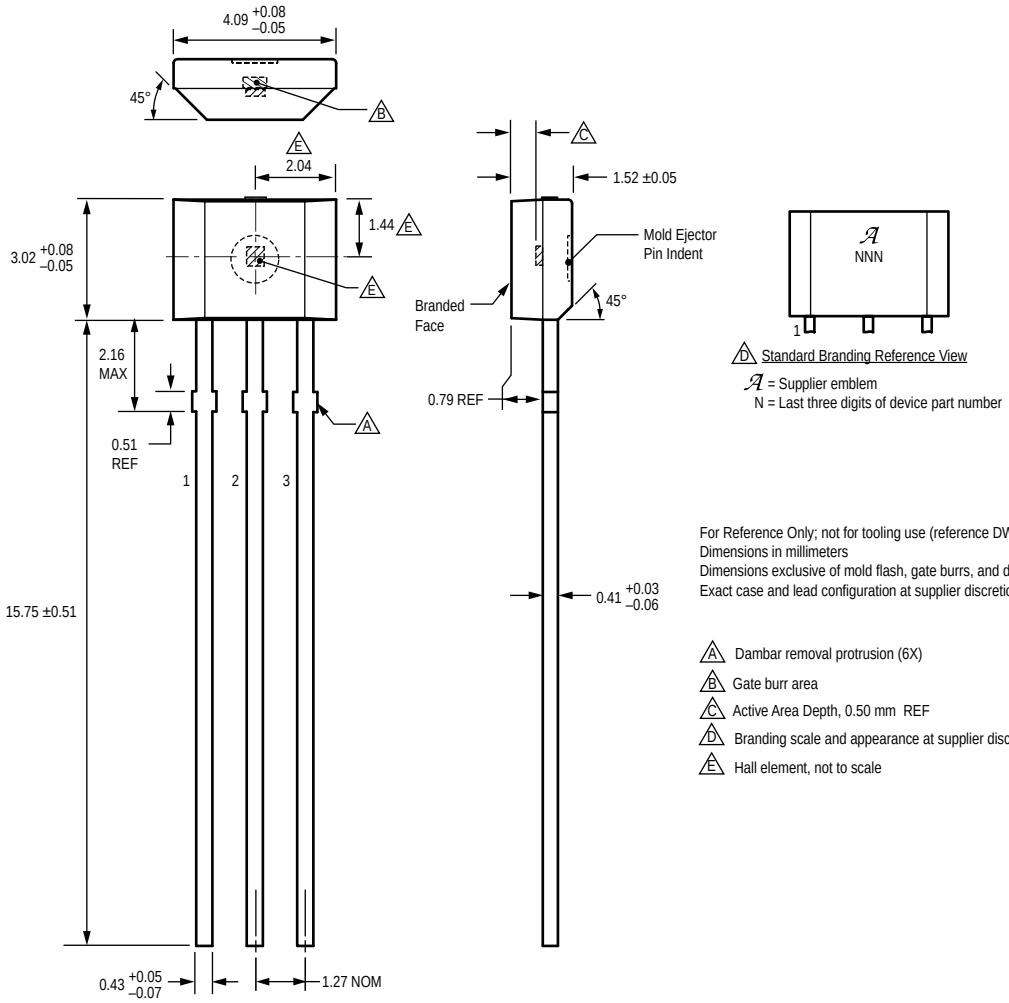
A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

Package UA, 3-Pin SIP



For Reference Only; not for tooling use (reference DWG-9049)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Dambar removal protrusion (6X)
B Gate burr area
C Active Area Depth, 0.50 mm REF
D Branding scale and appearance at supplier discretion
E Hall element, not to scale

Revision History

Revision	Revision Date	Description of Revision
Final	September 22, 2011	Final release

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www.allegromicro.com